

# **STACKED SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING**

**[0001]** This application claims priority under 35 U.S.C. § 119 of Korean Patent Application No. 2003-10761, which was filed on February 20, 2003, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

## **BACKGROUND OF THE INVENTION**

### **Field of the Invention**

**[0002]** The present invention relates to a semiconductor package and method for fabricating. More particularly, the present invention relates to a method for stacking semiconductor chips and forming a stacked semiconductor package including a plurality of semiconductor chips in one semiconductor package.

### **Description of the Related Art**

**[0003]** While semiconductor manufacturing technologies have improved the integrity and decreased the size of semiconductor devices, fabricating a semiconductor package can still be expensive and burdensome. In particular, in a wafer fabricating process, a large financial investment must be made for upgraded facilities and new equipment in addition to research costs. In the case of semiconductor memory devices, the process of upgrading from 64-megabit Dynamic Random Access Memory (DRAM) to 256-megabit DRAM can be costly when requiring a new wafer fabricating process.

**[0004]** Semiconductor manufacturers have introduced a method for fabricating a semiconductor package by placing a plurality of semiconductor chips into one semiconductor package. The process of a stacked semiconductor package includes stacking at least two semiconductor chips. The stacking of the semiconductor chips provides a solution to improving the integrity and performance of the semiconductor package without the need for fabricating an entirely new wafer. For example, the 256-megabit DRAM can be fabricated

by assembling the semiconductor package with four 64-megabit DRAM semiconductor chips.

**[0005]** In previous methods for fabricating a multi-chip semiconductor package, the semiconductor package is made by stacking multiple unit semiconductor chips on top of one another. One such method for fabricating a stacked semiconductor package is disclosed in US Patent No. 6,239,496 entitled "Package Having Very Thin Semiconductor Chip, Multichip Module Assembled By The Package And Method For Manufacturing The Same."

**[0006]** However, this type of multi-chip semiconductor package requires a new assembly method, new materials, and complex fabrication processes.

### SUMMARY OF THE INVENTION

**[0007]** The present invention provides a stacked semiconductor package and method of fabricating the same using conventional equipment and processes that allow for fabrication with reduced cost.

**[0008]** In one exemplary embodiment of the stacked semiconductor package, on a first semiconductor chip, a second semiconductor chip is stacked offset such that a portion of the first semiconductor chip is exposed. At least one first conductor electrically connects the exposed portion of the first semiconductor chip to the second semiconductor chip.

**[0009]** In one exemplary embodiment, the first conductor does not extend beyond a periphery of the first semiconductor chip.

**[0010]** In another exemplary embodiment, the first conductor electrically connects at least one bond pad on the first semiconductor chip with at least one bond pad on the second semiconductor chip, and a redistribution pattern electrically connects the bond pad on the second semiconductor chip to a differently positioned bond pad on the second semiconductor chip. This embodiment may further include a frame supporting a chip package structure formed of at least the first and second semiconductor chips. And at least one second conductor may electrically connect the differently positioned bond pad to the frame. In other embodiments, a plurality of first conductors and/or a plurality of second conductors exist.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0011]** The above features and other advantages of the present invention will become more apparent by describing exemplary embodiments in detail with reference to the accompanying drawings, in which:

**[0012]** FIG. 1 is a top view of a redistribution pattern on a semiconductor chip in a semiconductor chip package according to an embodiment of the present invention;

**[0013]** FIG. 2 is a side view of a stacked semiconductor package according to an embodiment of the present invention;

**[0014]** FIG. 3 is another side view of stacked semiconductor package according to an embodiment of the present invention; and

**[0015]** FIG. 4 is a top view of stacked semiconductor package according to an embodiment of the present invention.

### DETAILED DESCRIPTION OF THE INVENTION

**[0016]** Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. In the following drawings, like reference numerals identify similar or identical elements.

**[0017]** FIG. 1 is a top view of a redistribution pattern 206 on an upper surface of a semiconductor chip according to an embodiment of the present invention. The redistribution pattern 206 may be formed on any of the semiconductor chips within a stacked semiconductor package of an exemplary embodiment of the invention. As shown, a plurality of first bond pads 202 are formed along an edge of the semiconductor chip 200, 300, 400. A plurality of second bond pads 204 are formed along opposite edges of the semiconductor chip 200, 300, 400. The redistribution pattern 206 is a pattern of wires that electrically connects respective first bond pads 202 to respective second bond pads 204. In the exemplary embodiment of Fig. 1, a one-to-one correspondence exists between the first and second bond pads 202 and 204, but the present invention is not limited to this arrangement. Also, the redistribution pattern 206 may be changed to accommodate any location of the first or second bond pad 202 and 204. Namely, the present invention is not limited to the positions of the first and second bond pads 202 and 204

shown in Fig. 1. In one exemplary embodiment, the first bond pad 202 is formed by a flexible wire bonding process that is based on the location of the second bond pad 204. In creating the first bond pads 202, the redistribution pattern 206 and the second bond pads 204 are formed on a film located at the uppermost part of a semiconductor chip. Next, an insulating film, for example a polyimide film, is coated on the semiconductor chip on which the redistribution pattern 206 and the second bond pad 204 are formed. After that, the portion of the semiconductor chip where the bond pads are to be etched 208 is etched to expose the first 202 and second 204 sets of bond pads.

**[0018]** Referring to FIG. 2, the stacked semiconductor package 100 according to an exemplary embodiment of the present invention includes a frame 110, which may be a printed circuit board used for a Ball Grid Array (BGA) package or a flexible substrate (the flexible substrate is also referred to as an insulated wiring board). In an example of the present invention the stacked semiconductor package is a Chip Scale Package (CSP) or a Quad-Flat No-lead (QFN) semiconductor package. As shown, in an exemplary embodiment, the stacked semiconductor package 100 is mounted to the die pad 112 using an insulating adhesive tape 120. Here, the insulating adhesive tape 120 is attached to a rear surface of a wafer from which the first semiconductor chip 200 is formed before a sawing process of the stacked semiconductor package 100 fabrication process.

**[0019]** The frame 110 used in the QFN semiconductor package includes a die pad 112 and an inner lead 114. The die pad 112 represents a portion where a first semiconductor chip 200, middle semiconductor chips 300A, 300B and a fourth semiconductor chip 400 of the QFN semiconductor package are mounted within the package 100 fabrication process. The inner lead 114 represents a portion where the stacked semiconductor chip package 100 is electrically connected to the frame 110.

**[0020]** The stacked semiconductor package 100 according to an exemplary embodiment of the present invention comprises first wires 130, for example, bonding wires, for electrically connecting respective first bond pads of the lower semiconductor chip 200, the middle semiconductor chips 300A and 300B, and the upper semiconductor chip 400 to each other. A ball bonding

process is used to bond the first wires 130 to the first bond pads 202 on the exposed portion of the lower semiconductor chip 200, and a stitch bonding process is used to bond the first wires 130 to the first bond pads 202 of the middle and upper semiconductor chips 300A, 300B and 400.

**[0021]** The stacked semiconductor package 100 according to an exemplary embodiment of the present invention includes second wires 140, for example, bonding wires for electrically connecting the inner lead 114 of the frame 110 with respective second bond pads of the upper semiconductor chip 400.

**[0022]** Also the stacked semiconductor package 100 includes a sealing resin 150 for sealing the semiconductor chips 200, 300A, 300B, and 400, the wires 130 and 140, and a part of the frame 110. The sealing resin 150 may be an Epoxy Mold Compound (EMC).

**[0023]** As described in detail below with respect to Figs. 3 and 4, the semiconductor chips of FIG. 2 are stacked in an offset fashion in order to expose the first bond pads 202 on one edge of the first and middle semiconductor chips 200, 300A and 300B. The offset stacking of the semiconductor chips in the QFN configuration exposes the first bond pads 202, the semiconductor chips 200, 300A and 300B such that the conductors 130 may electrically connect the respective first bond pads 202 of the chips.

**[0024]** FIG. 3 is a side view of the stacked semiconductor package illustrated in FIG. 2, and FIG. 4 is a top view of the stacked semiconductor chip package in FIG. 2.

**[0025]** Referring to FIG. 3, in an exemplary embodiment of the present invention the lower, middle, and upper semiconductor chips 200, 300A, 300B, and 400 are mounted on the die pad 112 of the frame in a offset or stepped shape. This exposes an edge portion of the first and middle semiconductor chips 200, 300A and 300B such that the first bond pads 202 on one edge of each chip are exposed. As such, the first conductors 130 may electrically connect, for example by wirebonding, respective first bond pads 202 of the first, middle and upper semiconductor chips 200, 300A, 300B and 400 together. When, in an exemplary embodiment the first conductors 130 are wires, the connecting portion 132 of the first wires 130 on the middle and upper semiconductor chips 300A, 300B, and 400 are formed by performing a ball-bonding process or a stitch-bonding process.

**[0026]** As further shown in FIGS. 3 and 4, the second conductors 140 electrically connect respective second bond pads 204 of the upper semiconductor chip 400 to the connection unit of the frame 110, for example, the inner lead 114. Thus, the first wires 130 and the second wires 140 may be wire-bonded in different directions and location to use space efficiently. Also, the second bond pads 204 of upper semiconductor chip 400 and the first bond pads 202 of the lower, middle, and upper semiconductor chips 200, 300A, 300B, and 400 respectively, are exposed for the connection of the first and second wires 130 and 140.

**[0027]** To fabricate the stacked semiconductor package according to the present invention, the frame 110 is prepared along with the lower, middle, and upper semiconductor chips 200, 300A, 300B, and 400 by assuring the proper bond pad distribution prior to the process of stacking the semiconductor chips. Following these preparations, the lower, middle, and upper semiconductor chips 200, 300A, 300B, and 400 are mounted on the die pad 112 of the frame 110 in a stepped shape so that the first bond pads 202 are exposed as shown in FIGS. 3 and 4. The semiconductor chips are attached by insulating adhesive tape 120 attached on the bottom surfaces of the semiconductor chips 200, 300A, 300B, and 400.

**[0028]** Then, the second bond pads of the lower, middle, and upper semiconductor chips 200, 300A, 300B, and 400 are wire-bonded with each other by the first wires 130. The wire bonding process includes the ball-bonding process, which is generally performed on the first bond pads on an exposed portion of a lower semiconductor chip 200 and a stitch-bonding process, which is usually performed on the first bond pads 202 on the middle and upper semiconductor chips 300A, 300B and 400. In addition, the second bond pad's 204 of the upper semiconductor chip 400 and the connection unit such as the inner lead 114 of the frame 110 are wired-bonded by the second wires 140. The resultant bonded wires are sealed with a sealing resin 150, for example, an EMC as shown in FIG. 2. In the case where the frame 110 is a printed circuit board or an insulating wiring board, solder balls may be selectively attached thereto.

**[0029]** In an exemplary embodiment of the present invention the lower, middle and upper semiconductor chips 200, 300A, 300B, and 400 are semiconductor

devices of the same kind, for example, dynamic random access memories (DRAMs). However, different types of semiconductor devices can be used if necessary as well as a variable number of semiconductor chips within the package.

**[0030]** According to the present invention, the stacked semiconductor package is capable of performing with improved functionality within a minimal area. This can be realized by improving the stacking method of semiconductor chips and the wire-bonding method. Further, the stacked semiconductor package can be made with relative ease and the cost of equipment investment can be reduced since conventional equipment and processes are used.

**[0031]** While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention.